In The Claims:

Claims 1-16 (canceled)

Claim 17. (currently amended) A semiconductor interconnect structure, comprising:

a substrate;

a conductive structure over the substrate, wherein the conductive structure ~~having~~ has a top surface and a side surface;

a first dielectric layer over the conductive structure and the substrate, having first level air gaps therein, wherein the side surface of the conductive structure is surrounded by the first level air gaps and an upper portion of the side surface is surrounded by the first dielectric layer, wherein a top surface of the substrate not covered by the conductive structure is lower than an interface between the substrate and the conductive structure;

an etching stop layer over the first dielectric layer, wherein the etching stop layer is disposed over the first level air gaps; and

an opening disposed over the top surface and part of the upper portion of the side surface of the conductive structure, wherein the first level air gaps are isolated from the opening by the etching stop layer.

Claim 18. (original) The interconnect structure of claim 17, wherein the conductive structure comprises a aluminum, copper, tungsten, polysilicon, metal, and metal alloy thereof.

Claim 19. (original) The interconnect structure of claim 17, wherein the material of the first dielectric layer and the etching stop layer are different.

Claim 20. (original) The interconnect structure of claim 17, wherein the etching selectivity of the first dielectric layer with respect to the etching stop layer is substantially high.

Claim 21. (original) The interconnect structure of claim 17, wherein the first dielectric layer comprises silicon oxide.

Claim 22. (original) The interconnect structure of claim 17, wherein the first dielectric layer comprises doped oxide.

Claim 23. (original) The interconnect structure of claim 17, wherein the first dielectric layer is formed by using a plasma enhanced chemical vapor deposition method (PECVD).

Claim 24. (original) The interconnect structure of claim 17, wherein the etching stop layer comprises silicon nitrides.

Claim 25. (previously presented) The interconnect structure of claim 17, wherein the etching stop layer comprises silicon nitride, aluminum oxide, aluminum nitride, titanium oxide, silicon carbide, or aluminum silicate.

Claim 26. (original) The interconnect structure of claim 17, wherein the etching stop layer is formed by using a plasma enhanced chemical vapor deposition method (PECVD).

Claim 27. (original) The interconnect structure of claim 17, wherein the etching stop layer is formed by using a photo-induced chemical vapor deposition (PICVD).

Claim 28. (original) The interconnect structure of claim 17, further comprising a second dielectric layer disposed over the first dielectric layer and the etching stop layer, wherein the opening exposes the conductive structure through the first dielectric layer and the second dielectric layer.

Claim 29. (original) The interconnect structure of claim 28, wherein the second dielectric layer comprises silicon oxide.

Claims 30-31. (canceled)

Claim 32. (original) The interconnect structure of claim 17, wherein the width of the opening is substantially equal to the width of the conductive structure.

Claims 33-71 (canceled)

Claim 72. (currently amended) A semiconductor interconnect structure, comprising:

a substrate;

a pair of conductive structures over the substrate, wherein an air gap disposed between the conductive structures; and

a dielectric layer over the conductive structures, the dielectric layer having a stop layer disposed over the air gap, and a top surface of the substrate not covered by the conductive structures is lower than an interface between the substrate and the conductive structures, wherein the dielectric layer has an opening disposed over at least a portion of the conductive structure and at least a top portion of the stop layer, the opening being isolated from the air gap.

Claim 73. (original) The interconnect structure of claim 72, wherein the etching selectivity of the dielectric layer with respect to the stop layer is substantially high.

Claim 74 (canceled)

Claim 75. (currently amended) A semiconductor interconnect structure, comprising:

a substrate;

a pair of conductive structures over the substrate, wherein an air gap disposed between the conductive structures; ~~and~~

a dielectric layer over the substrate, having an air gap formed within, the air gap disposed between the conductive structures, and a top surface of the substrate not covered by the conductive structures is lower than an interface between the substrate and the conductive structures;

a stop layer disposed over the air gap; and

an opening disposed over at least part of the stop layer and at least part of the conductive layer, wherein the air gap is isolated from the opening.